UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
WILLIAMS, LAWRENCE B

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/904,432	RAGHAVAN, SREEN
	Examiner	Art Unit
	Lawrence B Williams	2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _11 July 2001_.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-52_ is/are pending in the application.
   4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) _1-8,10-20,27-40 and 43-52_ is/are rejected.
7) ☒ Claim(s) _9,21-26,41 and 42_ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on _07 Februrary 2000_ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☐ All b) ☐ Some * c) ☐ None of:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. _____.
    3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
       application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _1_.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1.   Figures 1A-1C should be designated by a legend such as --Prior Art-- because only that

which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37

CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application.

The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37

CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not

accepted by the examiner, the applicant will be notified and informed of any required corrective

action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2.   The specification has not been checked to the extent necessary to determine the presence

of all possible minor errors. Applicant's cooperation is requested in correcting any errors of

which applicant may become aware in the specification.

Claim Objections

3.   Claim 46 is objected to because of the following informalities: Examiner suggests

applicant insert "to" between coupled and receive in line 5 of the claim.. Appropriate correction

is required.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on
sale in this country, more than one year prior to the date of application for patent in the United States.

5.   Claims 1-6, 12, 15, 27, 29-31, 34, 36-37, 44-45 are rejected under 35 U.S.C. 102(b) as

being anticipated by Rowan et al. (WO 99/45683).

(1) With regard to claim 1, Rowan et al. discloses in Figs. 1, a communication

system, comprising: a transmitter (102), the transmitter coupled to receive N parallel bits of data

and transmit the N parallel bits of data into K frequency separated channels (110A-110N) on a

transmission medium (104), where N and K are integers; and a receiver (106) coupled to receive

data from the K frequency separated channels from the transmission medium and recover the N

parallel bits of data (pg. 3, line 22 –pg. 4, line 10).

(2) With regard to claim 2, claim 2 inherits all limitations of claim 1, above. Furthermore,

Rowan et al. also discloses in Fig. 2-5, wherein the transmitter comprises a bit allocation circuit

(200) that receives the N parallel bits of data and creates K subsets of data bits; and K

modulators, wherein each of the K modulators (330A-K) encodes one of the K subsets of the N

parallel bits of data and creates an output signal modulated at a carrier frequency associated with

one of the K frequency separated channels; and an adder (502) that receives the output signal

from each of the K modulators and generates a transmit sum signal (212) for transmission on the

transmission medium (pg. 6, line 28- pg. 7, line 21).

(3) With regard to claim 3, claim 3 inherits all limitations of claim 2 above. Furthermore,

Rowan et al. also discloses in Figs. 3, 5 wherein at least one of the K modulators includes a data

encoder (302A) that receives the one of the K subsets of the N parallel bits of data associated

with the at least one of the K modulators and outputs an encoded signal; a symbol mapper

(Though Rowan et al. is silent as to a symbol mapper, it is well known in the art that QAM

incorporate use of a symbol mapper) coupled to receive the encoded signal and output a symbol;

and an up-converter (500A-500K) coupled to receive symbols from the symbol mapper and

generate the output signal, wherein the up-converter (Fig. 8) outputs data at the carrier

frequency of one of the K frequency separate channels that corresponds with the at least one of

the K modulators (pg. 4, lines 1-10).

(4) With regard to claim 4, claim 4 inherits all limitations of claim 3. Furthermore,

Rowan et al. also discloses the system, further including a digital-to-analog converter coupled

between the symbol mapper and the up-converter (pg. 9, line 25-pg. 10, line 2).

(5) With regard to claim 5, claim 5 inherits all limitations of claim 3 above. Furthermore,

Rowan et al. also discloses in Fig. 4, wherein the data encoder is a trellis encoder (406).

(6) With regard to claim 6, Rowan et al. also discloses wherein the symbol mapper is a

QAM symbol mapper, which maps the encoded output signal into a symbol that includes an in-

phase signal and a quadrature signal (pg. 9, lines 17-24).

(7) With regard to claim 12, Rowan et al. also discloses wherein the transmission medium

is optical fiber and the transmitter includes an optical output device (pg. 5, lines 20-22; pg. 12,

lines 1-9).

(8) With regard to claim 13, Rowan et al. also discloses wherein a subset of bits at a

lower carrier frequency contains fewer bits than a subset of bits associated with a higher carrier

frequency (pg. 7, lines 4-21).

(9) With regard to claim 14, Rowan et al. also discloses wherein each of the K subsets of

data bits includes the same number of data bits (pg. 7, lines 22-27).

(10) With regard to claim 15, claim 15 inherits all limitations of claim 2 above.

Furthermore, Rowan et al. also discloses in Figs. 12, 13 wherein the receiver comprises: K

demodulators (1000A-K), each of the K demodulators coupled to receive a signal from the

transmission medium (712A-K), the signal being the transmit sum signal transmitted through the

transmission medium, and retrieving one of the K subsets of data bits; and a bit parsing circuit

(1003) that receives each of the K subsets of data bits from the K demodulators and reconstructs

the N data bits transmitted by the transmitter (pg. 15, lines 3-12).

(11) With regard to claim 19, claim 19 inherits all limitations of claim 15, above.

Furthermore, Rowan et al. also discloses in Figs. 9B, 11 wherein at least one of the K

demodulators comprises: a down-conversion circuit (912A) that receives the signal from the

transmission medium and generates a symbol by converting the signal at the carrier frequency

appropriate for the one of the K demodulators; an equalizer circuit (914A) coupled to receive the

symbol from the down-conversion circuit and create an equalized symbol; and a decoder (1100)

which receives the equalized symbol and retrieves the one of the K subsets of bits associated

with the at least one of the K demodulators.

(12) With regard to claim 20, Rowan et al. also discloses in Fig. 9B, an analog-to-digital

converter coupled between the down-converter and the equalizer (pg. 7, lines 4-21).

(13) With regard to claim 27, claim 27 inherits all limitations of claim 1, above as claim 27 cites the method of the system disclosed in claim 1. Furthermore, Rowan et al. discloses in Figs. 1-5, a method of communicating between components over a transmission medium, comprising: separating N bits into K subsets of bits; encoding each of the K subsets of bits to form encoded subsets of bits; mapping each of the K encoded subsets of bits onto a symbol set to generate a K symbols representing each of the K subsets of bits; up-converting each of the K symbols to form an up-converted signal at one of a set of K carrier frequencies; summing the up-converted signals representing each of the K subsets of bits to generate a transmit sum signal; and coupling the transmit sum signal to the transmission medium (pg. 5, lines 20- pg. 6, line 4).

(14) With regard to claim 28, Rowan et al. also discloses wherein symbols transmitted at lower carrier frequencies represent fewer bits than symbols transmitted at higher carrier frequencies (pg. 7, lines 4-21).

(15) With regard to claim 29, claim 29 inherits all limitations of claim 27, above. Furthermore, Rowan et al. discloses in Fig. 4, wherein encoding each of the K subsets of bits includes encoding at least one of the K subsets of bits with a trellis encoder.

(16) With regard to claim 30, Rowan et al. also discloses wherein mapping each of the encoded subsets of bits includes QAM mapping (pg. 9, line 17-24).

(17) With regard to claim 31, Rowan et al. also discloses the method further including converting the K symbols to analog signals (pg. 9, line 25 - pg. 10, line 2).

(18) With regard to claim 32, Rowan et al. also discloses in Fig. 9B, providing digital filtering prior to converting the K symbols to analog signals (pg. 7, lines 4-21).

(19) With regard to claim 33, Rowan et al. also discloses in Fig. 9B, providing analog digital filtering prior to converting the K symbols to analog signals (pg. 7, lines 4-21).

(20) With regard to claim 34, claim 34 inherits all limitations of claim 27 above. Furthermore, Rowan et al. also discloses receiving a receive sum signal from the transmission medium; down-converting the received sum signal into a set of K signals; equalizing each of the K signals to receive equalized symbols; decoding the equalized symbols to reconstruct the K subsets of bits; and parsing K subsets of bits into N bits (pg. 14, lines 1-21).

(21) With regard to claim 35, Rowan et al. also discloses wherein receiving the receive sum signal includes a differential signal from a copper transport medium (pg. 7, lines 4-21).

(22) With regard to claim 36, claim 36 inherits all limitations of claim 34 above. Furthermore, Rowan et al. also discloses wherein receiving the receive sum signal includes receiving an optical signal (abstract).

(23) With regard to claim 37, claim 37 inherits all limitations of claim 34 above. Furthermore, Rowan et al. also discloses wherein down-converting the received sum signal includes receiving a symbol transmitted at a corresponding carrier frequency (pg. 14, lines 7-15; 22, -29).

(24) With regard to claim 38, Rowan et al. also discloses providing automatic power control (pg. 7, lines 18-21).

(25) With regard to claim 39, Rowan et al. also discloses in Fig. 9B, the method further including analog-to-digital (918A) conversion.

(26) With regard to claim 40, Rowan et al. also discloses in Fig. 9B, anti-aliasing filtering prior to analog-to-digital conversion.

(27) With regard to claim 43, Rowan et al. discloses in Fig. 11, wherein decoding the equalized symbols includes trellis decoding and QAM decoding.

(28) With regard to claim 44, Rowan et al. also discloses in Figs. 1-5, a system for communication between components, comprising: means (200) for allocating N bits of input data into K subsets; means for encoding each of the K subsets (302); and means for transmitting each of the K subsets into one of K channels (claims 1, 7 and 8).

(29) With regard to claim 45, Rowan et al. also discloses in Fig. 10, means for receiving data from the K channels (1000A); means for retrieving the K subsets (1002); and means for retrieving the N data bits (1004).

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 7-8, 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rowan et al. (WO 99/45683) as applied to claims 1 and 4 above in view of Frenkel (US Patent 5,838,268).

(1) As noted above, Rowan et al. discloses all limitations of claim 4 above. He does not however disclose the system including a digital filter coupled between the symbol mapper and the digital-to analog converter.

However Frenkel teaches in Fig. 1, an apparatus and method for modulation and

demodulation system, which includes a digital filter, coupled between the symbol mapper and

the digital-to analog converter.

Therefore it would have been obvious to one skilled in the art to incorporate the invention

of Frenkel with that of Rowan et al. as a method of improved modulating and demodulating of

data (col. 2, lines 25-34).

(2) With regard to claim 8, Frenkel also discloses a low-pass filter (20) coupled between

the digital-to-analog converter (50) and the up converter (40) (col.14, lines 28-44).

(3) With regard to claim 10, Rowan et al. discloses wherein the transmission medium is a

copper backplane and the transmitter includes a differential output driver (col. 8, lines 39-51).

(4) With regard to claim 11, Rowan et al. also discloses wherein the transmission medium

is FR4 copper trace and the transmitter includes a differential output driver (col. 8, lines 39-51).

8.   Claims 16, 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rowan

et al. (WO 99/45683) as applied to claim 15 above in view of van Nguyen (US Patent 6,462,679

B1).

(1) With regard to claim 16, claim 16 inherits all limitations of claim 15 above. As noted

above, Rowan et al. discloses all limitations of claim 15. He does not however disclose wherein

the receiver further includes an input buffer coupled between the K demodulators and the

transmission medium.

However, van Nguyen discloses in Fig. 5, wherein the receiver further includes an input

buffer coupled (202) between a demodulator and the transmission medium.

Therefore it would have been obvious for one skilled in the art to combine the teaching so

van Nguyen with those of Rowan et al. as a method to store data long enough for clock

generation (col. 5, lines 27-44).

(2) With regard to claim 17, van Nguyen also discloses wherein the input buffer receives

a differential receive sum signal (col. 5, lines 5-26)

(3) With regard to claim 18, Rowan et al. also discloses the system incorporating an

optical signal (abstract).

9.   Claim 46-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rowan et al.

(WO 99/45683) in view of Widmer (US Patent 6,496,540 B1).

(1) With regard to claim 46, Rowan et al. disclose in Figs. 1, a transmitter portion (102),

the transmitter portion coupled to receive N parallel bits of data and transmit the N parallel bits

of data into a first set of K frequency separated channels (110A-110N) on a transmission

medium, where N and K are integers, and a receiver portion (106) coupled to receive data from a

second set of K frequency separated channels from the transmission medium and recover the N

parallel bits of data (pg. 3, line 22 –pg. 4, line 10).

Rowan et al. does not explicitly disclose the transmitter and receiver comprising a

transceiver chip. However, Widmer (US Patent 6,496,540 B1) discloses a transceiver chip for

parallel data transmission (col. 1, lines13-42). Therefore applying a transmitter and receiver on a

transceiver chip would not be considered novel especially in fiber-optical design.

(2) With regard to claim 47, claim 47 inherits all limitations of claim 46. Furthermore,

Rowan et al. also discloses wherein the first set of K frequency separated channels have

substantially identical carrier frequencies with the second set of K frequency separated

channels (pg. 7, lines 4-21).

(3) With regard to claim 48, Rowan et al. also discloses in Figs. 2-5, wherein the

transmitter comprises: a bit allocation circuit that receives the N parallel bits of data and creates

K subsets of data bits, and K modulators, (330A-K) wherein each of the K modulators encodes

one of the K subsets of the N parallel bits of data and creates an output signal modulated at a

carrier frequency associated with one of the first set of K frequency separated channels; and an

adder (502) that receives the output signal from each of the K modulators and generates a

transmit sum signal (212) for transmission on the transmission medium (pg. 6, lines 28 - pg. 7,

line 21).

(4) With regard to claim 49, Rowan et al. also discloses in Figs. 3, 5, wherein at least one

of the K modulators includes a data encoder (302A) that receives the one of the K subsets of the

N parallel bits of data associated with the at least one of the K modulators and outputs an

encoded signal; a symbol mapper (though Rowan et al. is silent as to a symbol mapper, it is well

known in the art that QAM incorporates the use of a symbol mapper) coupled to receive the

encoded signal and output a symbol; and an up-converter (500A-500K) coupled to receive

symbols from the symbol mapper and generate the output signal, wherein the up-converter (Fig.

8) outputs data at the carrier frequency of one of the K frequency separate channels that

corresponds with the at least one of the K modulators (pg. 4, lines 1-10).

(5) With regard to claim 50, Rowan et al. also discloses in Fig. 4, wherein the encoder is

a trellis encoder (406) and the symbol mapper is a QAM symbol mapper (pg. 9, lines 17-24).

(6) With regard to claim 51, Rowan et al. discloses in Figs. 12, 12, wherein the receiver

comprises: K demodulators (1000A-K), each of the K demodulators coupled to receive a signal

from the transmission medium (712A-K), the signal being the transmit sum signal transmitted

through the transmission medium, and retrieving one of the K subsets of data bits; a bit parsing

circuit (1003) that receives each of the K subsets of data bits from the K demodulators and

reconstructs the N data bits transmitted by the transmitter (pg. 15, lines 3-12).

(7) With regard to claim 52, claim 52 inherits all limitations of claim 51. Furthermore,

Rowan et al. discloses in Figs. 9B, 11, wherein at least one of the K demodulators comprises:

a down-conversion circuit (912A) that receives the signal from the transmission medium and

generates a symbol by converting the signal at the carrier frequency appropriate for the one of

the K demodulators; an equalizer circuit (914A) coupled to receive the symbol from the down-

conversion circuit and create an equalized symbol; and a decoder (1100) which receives the

equalized symbol and retrieves the one of the K subsets of bits associated with the at least one of

the K demodulators.

Allowable Subject Matter

10.   Claims 9, 21-26, 41-42 are objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims.

11.   The following is a statement of reasons for the indication of allowable subject matter:

The instant application discloses a communications method and system for high data rate

transmission. A search of prior art records has failed to disclose a method or system " wherein

the up-converter generates a first signal by multiplying the in-phase portion of the complex

symbol by a sine function of the carrier frequency, generates a second signal by multiplying the

out-of-phase portion of the complex symbol by a cosine function of the carrier frequency, and

summing the first signal with the second signal to generate the output signal " or "including an

anti-aliasing filter coupled between the down-converter and the analog-to-digital converter" as

taught in claims 9 and 21, respectively. The prior art also fails to teach "providing adaptively

controlled filtering for timing recovery" or "wherein the symbols are complex and further

providing adaptively controlled phase rotation as taught in claims 41 and 42.

Conclusion

12.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

     a.) Ziegler et al. discloses in US 2003/0112798 A1 a Data Communication Method.

     b.) Hendrickson et al. discloses in US 2002/0093994 A1 a Reverse Data De-Skew

Method and System.

     c.) Scott discloses in US Patent 4,710,992 Apparatus and Associated Methods For

Converting Serial Data Pattern Signals Transmitted or Suitable For Transmission Over a High

speed Synchronous Serial Transmission Media, To Parallel Pattern Output Signals.

     d.) Scott discloses in US Patent 5,079,770 Apparatus and Associated Methods For

Converting Serial Data Pattern Signals Transmitted or Suitable For Transmission Over a High

speed Synchronous Serial Transmission Media, To Parallel Pattern Output Signals.

     e.) Shimizu discloses in US Patent 5,293,378 Parallel Multi-Line Packet Transmission

System.

13.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037.

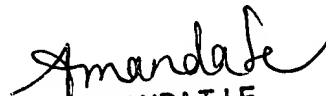The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
November 24, 2004

AMANDA T. LE
PRIMARY EXAMINER